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| EE260 Assignment 2 |

**Submitted by:**

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Grade:



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1. (5 pts) Problem 3.6 (a)-(b)
   1. 



1. (5 pts) Problem 3.7 (a)-(d)
   1. 
   2. 
   3. 
   4. 
2. (5 pts) Problem 3.9 (a)-(c)
   1. 
   2. 
   3. 
3. (5 pts) Problem 3.10 (a)-(c)
   1. 
   2. 
   3. 
4. (5 pts) Problem 3.21

We can write the it as n-input OR gate  using n=5 as ex.  (eq. 1). Using n=5 for a n-input OR gate and after reducing we get the same equation as equation 1  So that being said we can have a n-input OR gate and replace it by a (n-1) 2 input OR gates.

1. (10 pts) Simplify the following expressions using K-map:
   1. A’B’C’+A’BC’+A’B’C’+AB’C





* 1. A’B’C’D’+A’B’C’D+A’BCD’+AB’CD’+AB’CD+ABCD’+ABCD





1. (10 pts) Problem 3.37

A BUT gate if A1 and B1 are 1 Y1 is 1 but if either A2 or B2 is 0. Y2 is defined symmetrically. Making this table



This makes the minimal SOP for the BUT gate outputs by creating a K-map

Y1 K-map is



With the k-map a logical equation can be created



Now for the Y2 k-map



From this we get the logical equation for Y2

